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09/586,145	06/02/2000	Chris M Katsetos	24914-130A	6977

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EXAMINER	
GOSSAGE, GLENN A	
ART UNIT	**PAPER NUMBER**
2187	6

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,145	KATSETOS ET AL.	
	Examiner	Art Unit	
	Glenn Gossage	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-17,19-32 and 34-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-9, 34 and 35* is/are allowed.

6)☒ Claim(s) *10,11,13-17,19-32,36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The abstract of the disclosure is objected to because in lines 5-8, it appears "memory cache" should be --memory, such as a cache-- for clarity. In line 13, it appears "electronic" should be --electronics-- (note the amended paragraph starting on page 1).

Appropriate correction is required. See MPEP § 608.01(b).

2. The proposed drawing corrections filed on January 9, 2004 have been approved by the Examiner, subject to drafting review.

Applicant is REQUIRED to submit formal drawings incorporating the approved drawing corrections in response to this Office action.

3. It is once again noted that the disclosure has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

In the paragraph starting on page 1, line 3, at line 3 of the paragraph as amended, it appears "an" should be --a--.

In the paragraph starting on page 6, line 12, at line 3 of the paragraph, it appears "MFM" (first occurrence) should be deleted for clarity and consistency (see Figure 1).

In the paragraph starting on page 12, line 23, at line 3 of the paragraph, "complimentary" should be --complementary--.

On page 14, line 29, it appears "Hz" should be --Hertz (Hz)-- for clarity.

In the claims:

In claim 14, line 2, it appears --from the memory-- should be inserted after "stream" for consistency (note claim 10, line 6, e.g.).

Appropriate correction is required.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-11, 14-17, 21-24, 29-30 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (see page 1, line 6 to page 2, line 8 of the present specification, e.g.) in view of Kobayashi and Noll, taken together.

With respect to claims 10 and 16, applicants' admitted prior art discloses that various methods for writing and reading to and from storage devices such as hard drives in a computer system were well known in the art at the time the claimed invention was

made. The hard drives typically are manufactured to operate so as to be compliant with industry standards formats or protocols so as to be compatible with a large number of devices. However, the usefulness of controllers designed for older interfaces or standards such as the IEEE 412 or ST506 standard which utilizes a serial data stream has diminished as storage devices or hard drives complying with the newer ATA or IDE standard which use a parallel interface have gained wider acceptance (see page 1, line 6 to page 2, line 8, e.g.).

Kobayashi similarly discloses various methods for reading and writing data to and from devices such as hard drive controllers and storage devices, and teaches converting between a serial stream or standard and a parallel standard or protocol such as the ATA standard. Kobayashi discusses converting from a universal serial bus protocol to an ATA or IDE standard or protocol, but also discusses that the teachings are applicable with equal effect to the case where different serial and parallel standards are converted to each other, and is widely applicable to the case in which the peripheral equipment of the computer are controlled (see column 14, lines 11-20). Kobayashi also teaches that since many existing are based on the ATA standard, by converting between the serial protocol or standard of the controller or computer and the parallel ATA standard of the storage device, compatibility with existing devices may be maintained (see column 2, line 55 to column 3, line 19, as well as column 6, lines 14-17, and column 10, lines 15-20, e.g.).

Noll similarly discloses methods for reading and writing between devices utilizing different industry standards or protocols. Noll teaches that IDE drives which are

compliant with the ATA industry standard have achieved similar densities at similar access times than other industry standard drives, and also teaches that such IDE or ATA drives are typically cheaper and smaller than drives such as SCSI drives. Noll further teaches that it would be desirable to be able to connect an IDE hard drive with an older controller or bus standard to take advantage of the smaller size and lower price with comparable storage capacities and access times (see column 2, lines 45-53 and column 8, lines 1-6, e.g.). Noll also teaches utilizing a buffer or memory when interfacing the two different standards or when transferring data to and from the IDE drive (see column 8, lines 1-6, e.g.).

One of ordinary skill in the art at the time the claimed invention was made having the teachings of Kobayashi and Noll before him or her would have found it readily obvious to provide an interface and convert between a serial stream or standard and a parallel standard or protocol such as the ATA standard, as taught by Kobayashi, in a system having a controller utilizing serial data streams such as in applicants' admitted prior art, in order to provide compatibility with a large number of industry standard devices, particularly in light of the discussion in Kobayashi that the teachings are applicable with equal effect to the case where different serial and parallel standards are converted to each other, and is widely applicable to the case in which the peripheral equipment of the computer are controlled (see column 14, lines 11-20). While the internal details of the serial to parallel converter are not explicitly shown in Kobayashi, a serial-to-parallel converter which includes some storage device to quickly and easily perform serial to parallel conversion with a minimum number of components, and the synchronization of

a serial data stream to a clock were well known in the art at the time the claimed invention was made, official notice being hereby taken, and the use such circuitry to perform the well known serial to parallel conversion in the methods of applicants' admitted prior art in view of Kobayashi and Noll, taken together, as discussed above, would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made and, as such, does not render the claimed invention patentably distinct. That is, synchronizing a serial data stream to a clock and using a register or other storage device within the converter to store data while performing the conversion in the system of applicants' admitted prior art in view of Kobayashi et al and Noll in order to allow for simple data communication and transfer between devices would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made. The well known use of a memory or buffer in an interface so as to provide for different data rates between different devices or standards is taught by Noll (again see column 8, lines 1-6, e.g.), and the use of such a buffer or memory when converting data between a serial data stream and a parallel data stream such as in Kobayashi so as to provide for different data rates between the different devices or standards would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made.

With respect to claims 11 and 17, as well as claim 29, it would have been obvious to utilize an integrated device electronics (IDE) hard disk drive because of its wide industry acceptance and because Noll teaches that it would be desirable to be able to utilize an IDE hard drive to take advantage of the smaller size and lower price with comparable

storage capacities and access times. Similarly, the use of a converter with a serial data stream encoded according to the modified frequency modulation (MFM) specification would have been obvious since this standard or protocol was widely used in the industry and would provide for compatibility with a large number of devices.

With respect to claim 14, as well as claims 21 and 30, a processor or controller will read and write data during a time frame that is "convenient" for the processor. The data may be loaded from the hard drive to the buffer memory or cache without processor intervention. Note that Kobayashi teaches utilizing commands which may be processed uniquely by the converter (see column 3, lines 48-53, e.g.) so as to increase operating speed.

As per claims 15 and 24, it would have been obvious to perform coherency maintenance operations and write modified or "dirty" data from the memory to the component when the component is idle so as not to interfere with host access to the component (hard drive), thereby avoiding conflicts and the need for arbitrating access to the component (hard drive). An interrupt may be generated

With respect to claims 22 and 23, the data rates or clock frequency may obviously be adjusted and the selection of a particular speed or frequency does not render the claimed invention patentably distinct.

As per claim 29, data may be repeatedly out in the system of applicants' admitted prior art in view of Kobayashi and Noll as discussed above, with an index pulse being used to delineate the tracks of data consistent with serial data transfer from a disk having plural tracks in a well known manner.

With respect to claims 36 and 37, one of ordinary skill in the art would recognize that computer related inventions may be implemented in hardware and/or software and the use of a computer readable medium storing instructions for implementing the above methods would have been readily obvious to one of ordinary skill in the art.

5. Claims 13, 19-20, 25-28 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art (see page 1, line 6 to page 2, line 8 of the present specification, e.g.) in view of Kobayashi and Noll, taken together, as applied to claims 10-12, 14-18, 21-24, 29-30 and 36-37 above, and further in view of Weber et al.

With respect to claim 13, applicants' admitted prior art in view of Kobayashi and Noll, taken together, discloses an interface and methods for transferring data between devices having different industry standards or protocols including serial to parallel and parallel to serial conversion and a buffer memory (see numbered paragraph 7 above), but does not teach that the buffer used in conjunction with the serial to parallel and parallel to serial conversion is a cache buffer memory.

Weber et al similarly discloses an interface between a computer or controller including an interface using serial to parallel and parallel to serial conversion, and additionally teaches utilizing a cache buffer memory in the interface so as to provide fast access to the data stored in the cache memory in a well known manner (see cache 36 and interface 28 in Figure 1, e.g.). Weber et al also teaches using the cache buffer with well known industry standards or protocols such as ST506 or ST412 (also known as

IEEE 412) and IDE (see column 4, lines 1-6, e.g.). As one of ordinary skill in the art would appreciate, the use of a cache memory provides faster access to data stored therein so as to reduce overall access times and increase operating speed, and to prevent the controller or processor from experiencing excessive idle times due to differences in transfer rates, thereby increasing overall throughput (see column 1, lines 27-51, e.g.).

Accordingly, it would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made to utilize a cache buffer memory in conjunction with an interface between a disk drive and a controller, as taught by Weber et al, in the methods of reading and writing of applicants' admitted prior art in view of Kobayashi and Noll, taken together, as previously discussed, in order to reduce overall access times and increase operating speed, and to prevent the controller or processor from experiencing excessive idle times due to differences in transfer rates.

With respect to claims 19-20 and 31, Weber et al also teaches checking if there is a cache "miss" (determining whether data is "missing" from the cache) and loading data from the component (hard drive) to the cache when the data is "missing from the cache (see column 1, lines 41-54, e.g.). The data may be output "substantially" immediately after the data is found to be in the memory to reduce delays.

With respect to claims 25-26 and 28, it would have been obvious to utilize an integrated device electronics (IDE) hard disk drive because of its wide industry acceptance and because Noll teaches that it would be desirable to be able to utilize an IDE hard drive to take advantage of the smaller size and lower price with comparable

storage capacities and access times, as discussed above with respect to claims 11 and 17. Similarly, the use of a converter with a serial data stream encoded according to the modified frequency modulation (MFM) specification would have been obvious since this standard or protocol was widely used in the industry and would provide for compatibility with a large number of devices. Since MFM encoding and an ST506 or ST412 standard or protocol is being used, it would be necessary to use handshaking signals such as a seek complete signal or line for compliance with the protocol or standard.

With respect to claim 27, a processor or other controller may be used to transfer data between the component (hard drive) and the cache or buffer in a well known manner.

With respect to claims 32 and 33, Weber et al teaches writing data over or evicting data from the cache based on age (see column 5, lines 65-68, e.g.), and the use of a cache replacement scheme such as least recently used (LRU) to maintain the newest data in the cache memory would have been readily obvious to one of ordinary skill in the art.

6. Applicant's arguments filed January 9, 2004 have been considered but are not persuasive.

Initially, the response does not address the Examiner's contention that synchronizing a serial data stream to a clock and using a register or other storage device within a serial-parallel converter to store data while performing the conversion was well known in the art, and that use of such a well known serial-parallel converter in the system of applicants' admitted prior art in view of Kobayashi et al and Noll in order to perform the

conversions discussed in these references to allow for simple data communication and transfer between devices would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made.

Additionally, the argument that the references themselves do not provide any motivation or suggestion to combine the teachings contained therein is not persuasive Noll clearly teaches that it would be desirable to be able to utilize an IDE hard drive to take advantage of the smaller size and lower price with comparable storage capacities and access times. Kobayashi also teaches that since many existing devices are based on the ATA standard, by converting between the serial protocol or standard of the controller or computer and the parallel ATA standard of the storage device, compatibility with existing devices may be maintained (see column 2, line 55 to column 3, line 19, as well as column 6, lines 14-17, and column 10, lines 15-20, e.g.). Thus the Examiner respectfully submits that the references do provide ample motivation and suggestion to combine the teachings of the references to arrive at a structure on which applicants' claims read.

7. Claims 1-9, 34 and 35 are allowed over the prior art of record.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187